DOUBLE GATE STATIC INDUCTION THYRISTOR

This is a continuation, of application Ser. No. 132,002, filed Dec. 11, 1987, now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a double gate static induction thyristor, and more specifically to a buried-gate type and surface-wiring type double gate static induction thyristor and a manufacturing method therefor.

2. Description of the Related Art

The double gate static induction thyristors have already proposed and examined by various publications such as Japanese patent publication No. Sho 57-004100, U.S. Pat. No. 4,086,611, IEEE Trans. Electron Devices, vol. ED-22, No. 4, pp 185–195 (1975), IEEE Electron Device Letters vol. EDL-7, No. 3, pp. 175–178 (1986), and Japanese Patent Application Laid-open Nos. Sho 61-198776 and Sho 60-208873. This double gate static induction thyristor cannot only switch a large current at a very high speed, but also can be turned off by controlling the voltage of the gate, differently from conventional silicon controlled rectifiers.

FIG. 1 shows a schematic cross-sectional view of a typical example of the double gate static induction thyristors.

The shown thyristor is separated into an upper part and a lower part by a center p-n junction **6**. The upper part includes a p^--type semiconductor layer **5** contiguous to an n^--type semiconductor layer **4** of the lower part so as to form the p-n junction **6** therebetween. Another p^--type semiconductor layer **9** is formed on the layer **5**, and in addition, n^+-type gate regions **7** are formed at a periphery of the layer **5** and also between the layers **5** and **9** in the form of buried regions. An anode electrode **10** is deposited on the second p^--type layer **9**. Furthermore, an n^--type semiconductor layer **1** is formed on the n^--type layer **4**, and p^+-type gate regions **2** are formed at a periphery of the layer **4** and also between the layers **1** and **4** in the form of buried regions. In addition, a cathode electrode **11** is deposited on the second n^--type layer **1**, and gate electrodes **12** are deposited on the exposed gate regions **2** and **7**.

Incidentally, in this specification and in the attached drawings, "p^-" is used to mean that p-type impurities are included or doped at a low concentration, and "p^+" is used to mean that p-type impurities are included or doped at a high concentration. Further, "n^-" means that n-type impurities are included or doped at a low concentration, and "n^+" means that n-type impurities are included or doped at a high concentration.

With the above mentioned arrangement, if the gate electrodes **12** are suitable biased, a current will flow from the anode **10** to the cathode **11** through current paths **8** formed between the gate regions **7** and current paths **3** formed between the gate regions **2**, in such a manner that holes are injected from the anode **10** and electrons are injected from the cathode **11**.

As can be known from FIG. **1**, the conventional double gate static induction thyristor is such that the bottoms of all the p^+-type first gate regions **2** facing the p-n junction **6** substantially lie in a single flat plane, i.e., at the same level, and the bottoms of all the n^+-type second gate regions **7** facing the p-n junction **6** also substantially lie in another single flat plane, i.e., at the same level.

In order to manufacture such thyristors, the following two methods are widely used.

According to the first manufacturing method, a semiconductor substrate is prepared to constitute the n^--type semiconductor layer **1**. Then, the following operations are sequentially performed to the substrate **1**: On an upper principal surface, or a first surface, of the n^--type semiconductor substrate **1**, the p^+-type gate regions **2** are selectively formed; The n^--type semiconductor layer **4** is grown epitaxially on the upper principal surface of the n^--type semiconductor substrate **1** including the surface of the p^+-type gate regions **2**; The p^--type semiconductor layer **5** is epitaxially grown on the n^--type epitaxial layer **4**; The n^+-type gate regions **7** are selectively formed on the upper surface of the p^--type epitaxial layer **5**; The p^--type semiconductor layer **9** is epitaxially grown on the p^--type epitaxial layer **5** including the surface of the n^+-type gate regions **7**; The n^--type semiconductor substrate **1** is selectively etched to expose partially the first gate regions **2**; The p^--type semiconductor layer **9** is selectively etched to expose partially the second gate regions **7**; and the anode electrode **10**, the gate electrodes **12** and the cathode electrode **11** are formed on the p^--type epitaxial layer **9**, the first and the second gate regions **2** and **7**, and the n^--type semiconductor substrate **1**, respectively.

According to the other manufacturing method of the conventional double gate static induction thyristor, the p^--type semiconductor lower layer **5** is provided as a substrate. Then, the following operations are sequentially performed to the substrate **5**: On a lower principal surface of the p^--type semiconductor substrate **5**, the n^--type semiconductor layer **4** is epitaxially grown; On an upper principal surface of the p^--type semiconductor substrate **5**, the n^+-type gate regions **7** are formed; The p^--type semiconductor layer **9** is epitaxially grown on the substrate **5** including the n^+-type second gate region **7**; The p^--type gate regions **2** are formed on the lower surface of the n^--type epitaxial layer **4**; The n^--type semiconductor lower layer **1** is epitaxially grown on the n^--type epitaxial layer **4**; The n^--type semiconductor layer **1** is selectively etched to expose the first gate regions **2**; The p^--type semiconductor layer **9** is selectively etched to expose the second gate regions **7**; The anode electrode **10**, the gate electrodes **12** and the cathode electrode **11** are formed on the p^--type epitaxial layer **9**, the first and the second gate regions **2** and **7**, and the n^--type epitaxial layer **1**, respectively.

In the above mentioned static induction thyristor, as explained hereinbefore, a principal current flows through a principal current path formed between each pair of adjacent gate regions, i.e., through the channel regions **3** and **8**. In other words, a current does not flow in the gate regions. Therefore, in order to increase the current capacity of the thyristor, it is very important to make as small as possible the area of the shadow of the gate regions which is projected onto the cathode electrode **10** and the anode electrode **11** of the thyristor.

The static induction thyristor has a blocking characteristics which is greatly dependent upon the interval or space between each pair of adjacent gate regions. Namely, the blocking gain is smaller in a large gate interval portion than in a small gate interval portion. In addition, if the intervals between respective pairs of adjacent gate regions are not equal, the blocking volt-